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Sheet 1 of 2

FORM	PTO-1449	(SUBSTIT	UTE)	\

U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE

> INFORMATION DISCLOSURE STATEMENT BY APPLICANT (37 CFR 1.98(b))

Attorney Docket No.:

Applic. No.

L&L-10178

09/996,279

Applicant

Lothar Risch et al.

Filing Date

Group Art Unit

November 28, 2001

COPY OF PAPERS OFIGINALLY FILED

U.S. PATENT DOCUMENTS

EXAMINER INITIALS		PATENT NO.	DATE	PATENTEE	CLASS	SUB CLASS	FILING DATE
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		DOCUMENT NO.	DATE	COUNTRY	CLASS	SUB CLASS		NSL. NO
gn	J	44 33 086 C2	03/30/95	Germany				Х
	К	198 03 479 A1	12/24/98	Germany				Х
	L	0 612 103 A2	08/24/94	Europe			Х	
N	М	0 704 909 A2	04/03/96	Europe			Х	
	N							

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)

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Colinge, J.P. et al.: "Silicon-On-Insulator 'Gate-All-Around Device", IEDM 1990, pp. 595-598

Wong, Hon-Sum Philip et al.: "Self-Aligned (Top and Bottom) Double-Gates
MOSEET with a 25 nm Thick Silicon Channel" IEDM 1997 np. 427-430 MOSFET with a 25 nm Thick Silicon Channel", IEDM 1997, pp. 427-430

EXAMINER

DATE CONSIDERED

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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FORM PTO-1	449 (S	UBSTITUTE)	Attorney Docket No.: Applic. No.						
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